

EFFECTIVE: MAY 2003 CURRICULUM GUIDELINES

A.	Division:	Instructional		Eff	ective Date:		May 2003	
B.	Department / Program Area:	Computing Science		Rev	vision:	x	New Course:	
	i iografii i irea.	Computing Science		If F Rev	Revision, Section(s) vised: F, H, O, Q			
				Dat	e of Previous Revision	on:	August 4, 1997	
				Dat	e of Current Revision	n:	November 18, 2002	
C:	CMPT-150	D: In As	troduction to ssembly Prog	o Dig gram	ital Circuits and ming		E: 3	
	Subject & Cour	rse No.	Descriptive	e Tit	le	Sen	nester Credits	
F:	Calendar Descri	ption:						
	minimization u arithmetic logi commercial sof such as the 80 branching, sub	inimization using mapping techniques, asynchronous and synchronous circuits, flip-flops, memories, ithmetic logic units, controllers, and interfacing to computers. Designs are implemented using a ommercial software product. Assembly language for one or more microprocessors/microcontrollers ich as the 80x86, 68HC11, or the MicroChip PICMicro is introduced, including register transfer, canching, subroutines, and interfacing.						
G:	Allocation of Co / Learning Settin	ontact Hours to Type of In ags	struction H	H:	Course Prerequisite CMPT 110 with a	s: minimu	m grade of C	
	Primary Methods of Instructional Delivery and/or Learning Settings:			I: Course Corequisites: None				
	Lecture / Laboratory		J	Course for which this Course is a Prerequisite: CMPT 250				
	for each descript	Number of Contact Hours: (per week / semester for each descriptor)		K: Maximum Class Size:				
	Lecture Laboratory	3 hours / week 2 hours / week			Lecture 25 Laboratory 25	5		
	Number of Weel	ks per Semester: 14						
L:	PLEASE INDIC	CATE:						
	Non-Credi	t						
	College Cr	edit Non-Transfer						
	X College Cr	edit Transfer:						
	SEE BC TRANK	SEER GUIDE EOR TRAN	NSEED DET		(www.beest.be.cs)			
	SEE DU TRANSFER OUIDE FOR TRANSFER DETAILS (WWW.000at.00.0a)							

M: Course Objectives / Learning Outcomes: The student should be able to: Demonstrate an understanding of the logic blocks composing a microprocessor Appreciate, via comparisons, the architecture of microprocessors Demonstrate, by design and implementation, using a software simulator, gate level logic of • microprocessor components such as memory, ALU, and controller Understand, via use, data representation including numbers of various bases and characters Design and implement assembly language programs • Course Content: N: 1 **Data representation** 1.1 Number systems 1.1.1 Decimal, binary, octal, hexadecimal 1.1.2 one and two's complement arithmetic 1.2 **Character representation** 1.2.1 ASCII (others such as EBCDIC and Unicode may be introduced) 2 Gates and combinational circuits 2.1 Simplification techniques 2.1.1 **Boolean algebra** 2.1.2 Karnaugh maps 2.1.3 Brief survey of other (software) techniques 2.2 Circuits 2.2.1 **Decoders and multiplexers** 2.2.2 ALU 3 Memory and sequential circuits 3.1 flip-flops 3.2 registers 3.3 memory 3.4 counters and synchronous circuits sequential machines and controllers 3.5 4 **Computer architecture** 4.1 **Machine cycles** 4.1.1 Fetch-decode-execute-increment PC 4.1.2 instruction cycles and register transfer 5 **Comparison of microprocessor families** architecture 5.1 5.2 instruction sets 6 Assembly language programming 6.1 the assembler 6.2 data transfer and addressing modes CPU states, flags, and logical operations 6.3 6.4 branching and structured programming 6.5 subroutines and parameter passing 0: Methods of Instruction: There are three components to the course: lectures, labs., and assignments.

The lecture is used to introduce new material; usually via a sequence of theoretical concepts, examples, and practical considerations. The book is to be used as a close adjunct to the lecture notes and examples.

The two hour weekly lab. is used for the teaching and evaluation of circuit designs using the software product LogicWorks and also the evaluation of assembly language programs implemented by the student.

Assignments include data representation, logic designs using LogicWorks, and assembly language

	programming.						
P:	Textbooks and Materials to be Purchased by Students:						
	Malvino, Brown, <u>Digital Computer Electronics</u> , Macmillan/McGraw-Hill						
	Portfolio for logic design assignments						
	• Two 3 ¹ / ₂ " high density diskettes						
Q:	Means of Assessment:						
	Evaluation will be carried out in accordance with Douglas College Policy. The final grade will be calculated from a particular distribution from the range below. The exact distribution will be given to the student on the first day of classes along with the course outline.						
	Distribution Range:						
	labs. (12 to 14)	15% - 30%					
	assignments (4 to 6)	20% - 30%					
	tests (1 to 2) (a) 15% - 25% each final examination	15% - 50% 20% - 40%					
	class participation ₁	0% - 5%					
	Note #1: participation includes (but is not limited to) attendance and/or short pop-quizzes and/or handing-in (part-of) a homework assignment						
R:	Prior Learning Assessment and Recognition: specify whether course is open for PLAR						
	Not at this time						
Cours	se Designer(s):	Education Council / Curriculum Committee Representative:					

Dean / Director:

Registrar:

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